WE CLAIM:

1. A method for co-verifying a hardware simulation of a field-programmable-system-level integrated circuit (FPSLIC) and a software simulation of the field-programmable-system-level integrated circuit, comprising the steps of:

simulating in hardware a FPSLIC device;

generating, from the simulation in hardware, a simulator-port layout of the FPSLIC device;

simulating, with an instruction-set simulator, in software the FPSLIC device;

outputting register contents from the instruction-set software, from the simulation in software; and

verifying contents from the simulator-port layout with the register contents.

2. The method as set forth in claim 1, further including the steps of:

outputting peripheral contents from the instruction-set simulator, from the simulation in software; and

verifying contents from the simulator-port layout with the peripheral contents.

3. The method as set forth in claim 1, further including the steps of:

outputting UART contents from the instruction-set simulator, from the simulation in software; and

verifying contents from the simulator-port layout with

LAW OFFICES
DAVID NEWMAN
CHARTERED
ENTENNIAL SQUARE
P.O. BOX 2728
A PLATA, MD 20646
(301) 934-6100

the UART contents.

4. A system for co-verifying a hardware simulation of a field-programmable-system-level integrated circuit (FPSLIC) and a software simulation of the field-programmable-system-level integrated circuit, comprising:

a hardware simulator for simulating a FPSLIC device, with the hardware simulator having a simulator-port layout of the FPSLIC device;

a software simulator for simulating the FPSLIC device, with software simulator having an instruction-set simulator for outputting register contents; and

verification software for verifying contents from the simulator-port layout with the register contents.

5. The system as set forth in claim 4, with:

said instruction-set simulator outputting peripheral contents; and

said verification software for verifying contents from the simulator-port layout with the peripheral contents.

6. The system as set forth in claim 4, with:

said instruction-set simulator outputting UART contents; and

said verification software for verifying contents from the simulator-port layout with the UART contents.

LAW OFFICES
)AVID NEWMAN
CHARTERED
NTENNIAL SQUARE
P.O. BOX 2728
\ PLATA, MD 20646
(301) 934-6100